WHAT IS CLAIMED IS:

1. A circuit comprising:
a compare unit; and
a datapath, coupled to said compare unit, wherein said datapath comprises
a plurality of adder units,
a selection unit, coupled to said adder units, and
a plurality of clocked storage stages.

2. The circuit of claim 1, further comprising:
an adder unit, coupled to an output of said selection unit; and
a memory device, coupled to said compare unit and said adder unit.

3. The circuit of claim 2, wherein
a signal path is from an input of said compare unit to an output of said adder unit, and
at least one of said clocked storage stages is coupled in said signal path.

4. The circuit of claim 2, wherein
said adder units are coupled to inputs of said compare unit, and
said selection unit is coupled to an output of said compare unit.

5. The circuit of claim 4, wherein
at least one of said clocked storage stages are coupled at a one of an input to a one of said adder units and an output of said adder unit.

6. The circuit of claim 4, wherein
at least one of said clocked storage stages is coupled within at least one of a one of said adder units,

said compare unit and said selection unit.

7. The circuit of claim 2, wherein
said datapath is configured to receive a signal comprising a plurality of channels.

8. The circuit of claim 7, wherein
said channels are interlaced with one another.

9. The circuit of claim 2, further comprising:
a multi-stage clocked storage device, wherein
said multi-stage clocked storage device comprises a plurality of said clocked storage stages.

10. The circuit of claim 1, wherein
said adder units are coupled to inputs of said compare unit, and
said selection unit is coupled to an output of said compare unit.

11. The circuit of claim 10, wherein
at least one of said clocked storage stages are coupled at a one of an input to a one of said adder units and an output of said selection unit.

12. The circuit of claim 10, wherein
at least one of said clocked storage stages are coupled between said adder units and said selection unit.

13. The circuit of claim 10, wherein
a plurality of said clocked storage stages are coupled between said adder units and said selection unit.

14. The circuit of claim 12, wherein
at least one other of said clocked storage stages is coupled between said compare unit said selection

unit.

15. The circuit of claim 10, wherein
at least one of said clocked storage stages is coupled within at least one of a one of said adder units, said compare unit and said selection unit.

16. The circuit of claim 1, wherein
said datapath is configured to receive a signal comprising a plurality of channels.

17. The circuit of claim 16, wherein
said channels are interlaced with one another.

18. The circuit of claim 16, wherein
a number of said channels is equal to a number of said clocked storage stages.

19. The circuit of claim 1, further comprising:
a multi-stage clocked storage device, wherein
said multi-stage clocked storage device comprises a plurality of said clocked storage stages.

20. The circuit of claim 19, wherein
said multi-stage clocked storage device further comprises said clocked storage stages.

21. The circuit of claim 20, wherein
said multi-stage clocked storage device is coupled at one of an input to a one of said adder units and an output of said selection unit.

22. The circuit of claim 1, further comprising:
a plurality of programmable function blocks, wherein
at least one of the programmable function blocks is configured to implement said circuit.

23. A programmable logic device comprising the circuit of claim 1.

24. A method comprising:
producing a first sum from first data received at a first input of a plurality of inputs and second data received at a second input of said inputs;
producing a second sum from third data received at a third input of said inputs and fourth data received at a fourth input of said inputs;
producing a selected sum by selecting a one of said first sum and said second sum, wherein
said selected sum is provided at an output; and
performing a plurality of clocked storage operations on a signal, wherein
said signal is conveyed on a signal path between a one of said inputs and said output.

25. The method of claim 24, further comprising:
producing a first output by comparing said first sum and said second sum, wherein
said comparing controls said selecting.

26. The method of claim 25, further comprising:
producing an offset; and
producing a third sum from said offset and said selected sum, wherein
said third sum is provided at said output.

27. The method of claim 26, wherein said producing said offset further comprises:
producing a second output using said first sum and said second sum, wherein
said producing said offset is based on said second output.

28. The method of claim 24, further comprising:
receiving a data signal comprising a plurality of channels, wherein
a number of said channels is equal to a number of said clocked storage operations.

29. The method of claim 24, further comprising:
producing a plurality of sums, wherein
said producing said sums comprises producing said first sum and producing said second sum, and
said producing said selected sum further comprises selecting a selected one of said sums.

30. An apparatus comprising:
means for producing a first sum from first data received at a first input of a plurality of inputs and second data received at a second input of said inputs;
means for producing a second sum from third data received at a third input of said inputs and fourth data received at a fourth input of said inputs;
means for producing a selected sum comprising means for selecting a one of said first sum and said second sum, wherein
said selected sum is provided at an output; and
means for performing a plurality of clocked storage operations on a signal, wherein
said signal is conveyed on a signal path between a one of said inputs and said output.

31. The apparatus of claim 30, further comprising:
means for producing a first output comprising means for comparing said first sum and said second sum, wherein
said means for comparing controls said means for

selecting.

32. The apparatus of claim 31, further comprising:
means for producing an offset; and
means for producing a third sum from said offset and said selected sum, wherein
said third sum is provided at said output.

33. The apparatus of claim 32, wherein said means for producing said offset further comprises:
means for producing a second output using said first sum and said second sum, wherein
said means for producing said offset is configured to use said second output to produce said offset.

34. The apparatus of claim 30, further comprising:
means for receiving a data signal, wherein
said data signal comprises a plurality of channels,
said channels are interlaced with one another, and
a number of said channels is equal to a number of said clocked storage operations.

35. The apparatus of claim 30, further comprising:
means for producing a plurality of sums, wherein
said means for producing said sums comprises said means for producing said first sum and said means for producing said second sum, and
said means for producing said selected sum further comprises means for selecting a one of said sums.